

In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

- 1 1. (currently amended) An integrated circuit, comprising:
 - 2 a configurable logic array having a programmable configuration defined by configuration
 - 3 data stored in electrically programmable configuration points within the configurable logic array;
 - 4 a programmable non-volatile configuration memory, adapted to store the configuration
 - 5 data;
 - 6 memory storing instructions for a mission function for the integrated circuit, [[and]]
 - 7 storing instructions for a configuration function used to transfer the configuration data from the
 - 8 programmable non-volatile configuration memory to the programmable configuration points
 - 9 within the configurable logic array;
 - 10 memory protected from overwriting or modification by an in circuit programming
 - 11 function and storing instructions for a configuration load backup function used to recover from
 - 12 an incomplete transfer of the configuration data from the programmable non-volatile
 - 13 configuration memory to the programmable configuration points within the configurable logic
 - 14 array; and
 - 15 a processor coupled to the memory which fetches and executes said instructions from the
 - 16 memory.
- 1 2. (original) The integrated circuit of claim 1, wherein said memory comprises a non-volatile
- 2 store.
- 1 3. (original) The integrated circuit of claim 1, wherein said memory comprises a floating gate
- 2 memory store.
- 1 4. (original) The integrated circuit of claim 1, wherein said memory comprises a read-only
- 2 memory store.

- 1 5. (original) The integrated circuit of claim 1, wherein said memory comprises a first non-
2 volatile store for the configuration function, and a second store for the mission function.
- 1 6. (original) The integrated circuit of claim 1, wherein said memory comprises a first volatile
2 store for the configuration function, and a second store for the mission function.
- 1 7. (original) The integrated circuit of claim 1, including a watchdog timer coupled to the
2 processor, and wherein the configuration function includes using the watchdog timer.
- 1 8. (previously presented) The integrated circuit of claim 1, wherein the configuration function
2 includes loading the programmable non-volatile configuration memory via an input port on the
3 integrated circuit.
- 1 9. (previously presented) The integrated circuit of claim 1, wherein the configuration function
2 includes receiving encrypted configuration data via an input port on the integrated circuit,
3 decrypting the configuration data, and loading the programmable non-volatile configuration
4 memory with decrypted configuration data.
- 1 10. (previously presented) The integrated circuit of claim 1, wherein the configuration function
2 includes receiving compressed configuration data via an input port on the integrated circuit,
3 decompressing the configuration data, and loading the programmable non-volatile configuration
4 memory with decompressed configuration data.
- 1 11-12. (canceled).
- 1 13. (original) The integrated circuit of claim 1, wherein the electrically programmable
2 configuration points comprise non-volatile, charge programmable memory cells.
- 1 14. (previously presented) The integrated circuit of claim 1, wherein the configuration function
2 includes loading the programmable non-volatile configuration memory via an input port on the
3 integrated circuit, and including:

4 an interface between the processor and the programmable non-volatile configuration
5 memory supporting said loading; and

6 an interface between the programmable non-volatile configuration memory and the
7 configurable logic array supporting said transfer of configuration data to the configurable logic
8 array.

1 15. (previously presented) The integrated circuit of claim 1, wherein the configuration function
2 includes loading the programmable non-volatile configuration memory via an input port on the
3 integrated circuit, and including:

4 an interface between the processor and the programmable non-volatile configuration
5 memory supporting said loading and said transfer of configuration data to the configurable logic
6 array; and

7 an interface between the processor and the configurable logic array supporting said
8 transfer of configuration data to the configurable logic array.

1 16. (previously renumbered as 15).

1 17. (canceled).

1 18. (previously presented) The integrated circuit of claim 1, wherein the interface between the
2 programmable non-volatile configuration memory and the configuration logic array comprises a
3 dedicated data path for said transfer of configuration data to the programmable logic array.

1 19. (previously presented) The integrated circuit of claim 1, wherein the interface between the
2 programmable non-volatile configuration memory and the configuration logic array comprises a
3 data path including the processor for said transfer of configuration data to the programmable
4 logic array.

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